After the collected profile packet is stored at the location indicated by R15, R15 is postincremented by the size of a profile packet.--.

At page 104, line 11, replace "tapestry" with --Tapestry--.

At page 110, line 12, replace "EPC" with --EPC.EIP--.

At page 110, line 20, replace "set" with --cleared--.

At page 117, line 29, replace "set" with --cleared--.

At page 118, line 30, replace "32" with --thirty-two--.

At page 130, line 21, replace "tapestry" with --Tapestry--.

In the claims:

Kindly amend the claims as follows.

1. (amended) A microprocessor chip, comprising:

instruction pipeline circuitry;

[address translation circuitry;] and

table lookup circuitry designed to index into a table, each entry of the table [having an entry] being associated with a [each] corresponding address range translated by [the] address translation circuitry of the microprocessor chip, each entry describing a likelihood of the existence of an alternate coding of instructions located in the respective corresponding address range, [the table lookup circuitry further designed to retrieve a table entry corresponding to the address,] the table lookup circuitry operable as part of the basic instruction cycle of executing an instruction of a non-supervisor mode program executing on a computer;

interrupt circuitry cooperatively designed with the instruction pipeline circuitry to trigger an interrupt on execution of an instruction of a process, synchronously based at least in part on a memory state of the computer and the address of the instruction, the architectural definition of the instruction not calling for an interrupt, a handler for the interrupt being responsive to the contents of the table to affect the instruction pipeline circuitry to effect control of an architecturally-visible data manipulation behavior or control transfer behavior of the instruction based on the contents of a table entry associated with the address range in which the instruction lies.

2. (amended) A method, comprising the steps of:

as part of the basic instruction cycle of executing an instruction of a non-supervisor mode program executing on a computer, consulting a table, the table being addressed by the address of instructions executed, for attributes of the instructions;

controlling an architecturally-visible data manipulation behavior or control transfer behavior of the instruction based on the contents of a table entry associated with the address of the instruction.

10. (amended) A microprocessor chip, comprising:

instruction pipeline circuitry;

table lookup circuitry designed to index into a table by a memory address of a memory reference arising during execution of an instruction, and to retrieve a table entry corresponding to the address, the table entry being distinct from the memory referenced by the memory reference;

the instruction pipeline circuitry being responsive to the contents of the table to alter [affect] a manipulation of data or transfer of control behavior of the instruction in a manner incompatible with the architectural definition of [defined for] the instruction.

Kindly add the following new claims.

24. (new) A method, comprising the steps of:

as an integral part of processing an instruction in instruction pipeline circuitry of a computer, consulting a lookup structure of entries, each entry corresponding to an address range translated by address translation circuitry, the entry describing a likelihood of the existence of an alternate coding of instructions located in the respective corresponding address range.

25. (new) The method of claim 24, further comprising the step of:

as a result of the consulting, changing an instruction set architecture under which instructions are interpreted by the computer.

26. (new) The method of claim 16.24, further comprising the step of:

altering a behavior of the instruction in a manner incompatible with the architectural definition of the instruction, based on the contents of the entry corresponding to the address range containing the instruction.

27. (new) The method of claim 24,

wherein each entry corresponds to a page managed by a virtual memory manager, circuitry for locating an entry being integrated with virtual memory address translation circuitry of the computer.

28. (new) The method of claim 24, further comprising the step of:

based on the contents of the entry, transferring control to an instruction flow of the process other than the instruction flow triggering the consulting, the returned-to instruction flow being programmed to carry on non-error handling normal processing of the process.

29. (new) The method of claim 24, further comprising the step of:

based on the contents of the entry, synchronously triggering an interrupt based at least in part on a memory state of the computer and the address of the instruction, wherein the architectural definition of the instruction does not call for an interrupt.

30. (new) A method, comprising the steps of:

on execution of an instruction of a process, the architectural definition of the instruction not calling for an interrupt, synchronously triggering an interrupt based at least in part on a memory state of the computer and the address of the instruction.

31. (new) The method of claim 30, further comprising the step of:

servicing the interrupt and returning control to an instruction flow of the process other than the instruction flow triggering the interrupt, the returned-to instruction flow being programmed to carry on non-error handling normal processing of the process.

32. (new) The method of claim 31, further comprising the step of: